VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a polarity switch comprising (i) a first memory cell connected to an input terminal of a [number of] first transmission [gates] gate and (ii) a second memory cell connected to an input terminal of a second transmission gate, wherein an input signal of said polarity switch is presented to a first control terminal of said first and said second transmission gates and an output of said polarity switch [selectably presents] is configurable in response to contents of said first and second memory cells to present either (i) a signal that varies in response to [a control] said input signal or (ii) a predetermined logic level that is independent of said [control] input signal.

2. (AMENDED) The apparatus according to claim 1, wherein said [number of] first and second transmission gates [is two] further comprise a second control terminal configured to receive a complement of said input signal.

3. (AMENDED) The apparatus according to claim 1, wherein said [output signal is selected in response to] first and second memory cells comprise a first configuration [signal] bit and a second configuration [signal] bit of said apparatus.

4. (AMENDED) The apparatus according to claim 1, wherein [further comprising a first storage element connected to] an [input] output terminal of [a] said first transmission gate and [a second storage element connected to] an [input] output terminal of [a] said second transmission gate are connected to said output of said polarity switch.

5. (AMENDED) The apparatus according to claim 1, wherein said [control] input signal [is] comprises an input term and said output is configured to present a product term input.

6. (AMENDED) An apparatus comprising:

a first circuit configured to present a first [stored] value stored in a first memory cell to an input node in response to a first state of [a control] an input signal; and

a second circuit configured to present a second [stored] value stored in a second memory cell to said input node in response to a second state of said [control] input signal, wherein said first and said second stored values are programmable during configuration of said apparatus.

7. (AMENDED) The apparatus according to claim 6, wherein said first and second circuits each comprise said first and second memory cells coupled to an input terminal of a first and a

second transmission gates, respectively, and said input signal is coupled to a control terminal of said transmission gates.

9. (AMENDED) The apparatus according to claim [6] 7, wherein said first and second circuits further comprise a [first and second storage element, respectively] first and a second CMOS inverters coupling said first and second memory cells to said first and second transmission gates.

10. (AMENDED) The apparatus according to claim [9] 7, wherein said output of said apparatus presents (i) a predetermined logic level when said memory cells of said first and said second [storage elements] circuits contain the same data and (ii) a signal that varies in response to said input signal when said memory cells contain [or] different data.

12. (AMENDED) The apparatus according to claim [9] 7, wherein said [first and second storage elements are] memory cells are configured to source [or] and sink a current.

15. (AMENDED) The apparatus according to claim 6, wherein said [control] input signal comprises an input term.

16. (AMENDED) The apparatus according to claim 15, wherein said apparatus is [programmed] programmable to present any of (i) said input term, (ii) a digital complement of said input term, [or] and (iii) a predetermined logic level to said input node.

17. (AMENDED) The apparatus according to claim 16, wherein said predetermined logic level is selectable from a digital 0 [or] and a digital 1.

18. (AMENDED) A method for providing a product term input of a programmable logic device comprising the steps of:

(A) presenting a first [stored] value stored in a first memory cell to an input node in response to a first state of [a control] an input signal; and

(B) presenting a second [stored] value stored in a second memory cell to said input node in response to a second state of said [control] input signal, wherein said first and said second stored values are programmed during configuration of said programmable logic device.

19. (AMENDED) The method according to claim 18, wherein said [control] input signal comprises an input term of a logic block of said programmable logic device.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a polarity switch comprising (i) a first memory cell connected to an input terminal of a first transmission gate and (ii) a second memory cell connected to an input terminal of a second transmission gate, where an input signal of the polarity switch is presented to a first control terminal of the first and the second transmission gates and an output of the polarity switch is configurable in response to contents of the first and the second memory cells to present either (i) a signal that varies in response to the input signal or (ii) a predetermined logic level that is independent of the input signal.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 6-10 and in the specification as originally filed, for example, on page 2, lines 1-7, on page 10, line 15 through page 12, line 18, on page 14, lines 3-18 and on page 15, lines 3-16. As such, no new matter has been added.

IN THE DRAWINGS

The objection to the drawings has been, in part, obviated and is, in part, respectfully traversed. FIGS. 1 and 2 have been labeled "conventional" in order to further the prosecution of the present application. Applicant's representative respectfully traverses the requirement to label FIGS. 3-5 as prior art. No admission has been made regarding FIGS. 3-5 as prior art. Furthermore, the Office Action does not present any evidence or convincing line of reasoning for considering the FIGS. 3-5 to be prior art (see page 2, paragraph no. 1 of the Office Action).

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(e) as being anticipated by Sako '914 has been obviated by appropriate amendment and should be withdrawn.

Sako is directed to a semiconductor integrated circuit capable of realizing logic functions (Title). Assuming, *arguendo*, the element TU of FIG. 13 of Sako is similar to the presently claimed polarity switch (as suggested on page 2, last two lines through page 3, line 8 of the Office Action and for which Applicant's representative does not necessarily agree), Sako does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the

presently claimed invention is fully patentable over Sako under 35 U.S.C. §102(e) and the rejection should be withdrawn.

Specifically, Sako does not disclose or suggest a polarity switch comprising (i) **a first memory cell connected to an input terminal of a first transmission gate** and (ii) **a second memory cell connected to an input terminal of a second transmission gate**, as presently claimed. For example, Sako shows that the input terminals (A and B in FIG. 13 of Sako) of the transmission gates in the element TU of Sako (transistors M1-M3 and M2-M4 in FIG. 13 of Sako) can be connected to an external interconnection element (i.e., L0-Lk) or a power supply voltage (i.e., GND or VDD) via an array of anti-fuses (see FIGS. 8 and 9 and column 22, line 50 through column 24, line 12 of Sako).

In contrast, the presently claimed invention (claim 1) provides a polarity switch comprising (i) **a first memory cell** connected to an input terminal of a first transmission gate and (ii) **a second memory cell** connected to an input terminal of a second transmission gate. Claims 6 and 18 include similar recitations. Because Sako does not disclose or suggest a polarity switch comprising **a first memory cell** connected to an input terminal of a first transmission gate and **a second memory cell** connected to an input terminal of a second transmission gate, as presently claimed, it follows that Sako does not disclose or suggest each and every element of the presently claimed invention,

arranged as in the present claims. As such, the presently claimed invention is fully patentable over Sako and the rejection should be withdrawn.

Claims 2-5, 7-17 and 19-20 depend, either directly or indirectly, from claims 1, 6 or 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over Sako and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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